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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,750	07/13/2001	Christopher W. Jones	0325.00485	3331

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CHRISTOPHER P. MAIORANA, P.C.
24840 HARPER
ST. CLAIR SHORES, MI 48080

EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	4

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,750	JONES ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan (US Patent 6,545,505) in view of Rangasayee (US Patent 6,404,225)

As per claims 1, 11, Chan discloses a device comprising:

- An assembly apparatus; (fig.2, CPLD 100)
- A programmable logic device(CPLD) mounted to said assembly apparatus and comprising (i) a plurality of logic block clusters[0069] and (ii) a plurality of routing channels configured to interconnect said logic block clusters; and (col.3, lines 12-21)

Chan discloses all the limitations as above except the communication channel to convert between a serial data signal and parallel data signal. However, Rangasayee discloses an embedded array type programmable logic architecture configured to operate as a serial to parallel signal converter. A serial signal includes data packets and supplied to PLD row I/O. (col.8, lines 13-28)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate

Rangasayee's teaching into Chan's system so as to increase flexibility enables the CPLD to fit more complex logic functions more often than possible with conventional CPLD architectures. (col.3, lines 47-50)

As per claim 2-5, 10, Chan discloses all the limitations as above except wherein (i) said die further comprises a second communication channel configured to convert between a serial data signal and a parallel data signal and (ii) coupled to said routing channels to exchange said parallel data signal with at least one of said logic block clusters. However, Rangasayee discloses an embedded array type programmable logic architecture configured to operate as a serial to parallel signal converter. A serial signal includes data packets and supplied to PLD row I/O. (col.8, lines 13-28)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Rangasayee's teaching into Chan's system so as to increase flexibility enables the CPLD to fit more complex logic functions more often than possible with conventional CPLD architectures. (col.3, lines 47-50)

As per claim 6, Chan discloses wherein said first communication channel is further coupled to said first routing channel to receive a control signal from one of said logic block clusters.(col.7, lines 25-44)

As per claim 7, Chan discloses wherein said control signal is configured as one of (i) a portion of said first parallel signal and (ii) an encoding selection signal. (col.7, lines 25-44)

As per claim 8, Chan discloses wherein said first communication channel is further coupled to said first routing channel to present a status signal to at least one of said logic block clusters. (col.7, lines 25-44)

As per claim 9, Chan discloses wherein said status signal is configured as one of (i) a portion of said first parallel signal and (ii) a special character indicator. (col.7, lines 25-44)

As per claim 12, Chan discloses the method further comprising the step of coupling a second communication channel of said die to a second of said routing channels to exchange a second parallel data signal between at least one of said logic block clusters and said second communication channel. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 13, Chan discloses the method further comprising the step of coupling a third communication channel of said die to a third of said routing channels to exchange a third parallel data signal between at least one of said logic block clusters and said third communication channel. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 14, Chan discloses the method further comprising the step of coupling a fourth communication channel of said die to a fourth of said routing channels to exchange a fourth parallel data signal between at least one of said logic block clusters and said fourth communication channel. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 15, Chan discloses the method further comprising the step of coupling a second communication channel of said die to said first routing channel to exchange a second parallel data signal between at least one of said logic block clusters and said second communication channel. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 16, Chan discloses the method further comprising the step of coupling said first receive channel to said first routing channel to receive a control signal from one of said logic block clusters. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 17, Chan discloses the method further comprising the step of coupling said first receive channel to said first routing channel to present a status signal to at least one of said logic block clusters. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 18, Chan discloses the method further comprising the step of coupling a second receive channel of said die to said first routing channel to receive a control signal from one of said logic block clusters. (col.7, lines 25-44), (col.5, lines 17-31)

As per claim 19, Chan discloses a circuit comprising:

- Means for mounting a first programmable die and a second die; (col.4, lines 58-67)
- Means for routing signals among a plurality of logic block clusters in said first programmable die; (col.4, lines 58-67)
- Means for converting between a first parallel data signal and a first serial data signal in said second die; and
- Means for coupling said means for converting to said means for routing to exchange said first parallel data signal between said means for converting and at least one of said logic block clusters. (col.5, lines 17-31)

Chan discloses all the limitations as above except the communication channel to convert between a serial data signal and parallel data signal. However, Rangasayee discloses an embedded array type programmable logic architecture configured to operate as a serial to parallel signal converter. A serial signal includes data packets and supplied to PLD row I/O. (col.8, lines 13-28)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Rangasayee's teaching into Chan's system so as to increase flexibility enables the CPLD to fit more complex logic functions more often than possible with conventional CPLD architectures. (col.3, lines 47-50)

Response to Amendment

3. Applicant's amendment filed on 3/10/04 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

4.. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

May 16, 2004

Khanh Dang
Primary Examiner